REMARKS

Claims 1 and 7 have been amended to differently recite the invention. Claims 1-7 are now pending.

In the pending Office Action, the Examiner objected to claim 7; rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by <u>Iwata</u> (JP 11-186593); rejected claim 2 under 35 U.S.C. 103(a) as being unpatentable over <u>Iwata</u> in view of <u>Niki et al.</u> (U.S. Patent No. 6,674,098); and rejected claims 1 and 3-7 under 35 U.S.C. 103(a) as being unpatentable over <u>Kondo et al.</u> (U.S. Published Patent Application No. 2004/0061054). Applicants traverse these objections and rejections, at least for the following reasons.

Applicants have amended claim 1 to correct the dependency irregularity noted in the Office Action. Reconsideration and withdrawal of the objection to claim 7 is respectfully requested.

To the extent any subsequent Office Action relies on Kondo et al., Applicants respectfully request that the Examiner identify the section of 35 U.S.C. 102 under which Kondo et al. is believed to constitute prior art. Kondo et al. is certainly not prior art under 35 U.S.C. 102(b), for example, and to the extent the Examiner is alleging that Kondo et al. constitutes prior art under 35 U.S.C. 102(e), Applicants respectfully request the Examiner to comment on how Kondo et al. meets each and every requirement of 35 U.S.C. 102(e).

Applicants traverse the art rejections applied to the claims. In this regard, Applicants submit that the applied references do not disclose or suggest any of Applicants' claimed combinations including an illuminant comprising a substrate and a nitride semiconductor layer

having a quantum well structure provided on and in direct contact with one surface of the substrate while covering the entire one surface of the substrate.

Iwata, for example, teaches a semiconductor light-emitting device with semiconductor thin chips 14 each having a structure such that cladding layers 12 sandwich an active layer 13 having a quantum well. Nonetheless, these semiconductor thin chips 14 do not cover the entire surface of the alleged substrate as is required by Applicants' claims. For at least this reason, Applicants submit that claim 1 and its dependent claims 2-7 patentably distinguish over Iwata.

Applicants also submit that neither <u>Kondo et al.</u> nor <u>Niki et al.</u> make up for the deficiencies in <u>Iwata</u>. As one example, Applicants submit that <u>Iwata</u> and <u>Kondo et al.</u> are not combinable in the manner asserted in the pending Office Action.

In this regard, claim 1 of the instant application recites an illuminant provided with a nitride semiconductor layer that emits fluorescence, which in turn can provide an efficient luminous intensity. Moreover, claim 1 of the instant application is characterized in that a quantum well is formed in the nitride semiconductor layer, which in turn can provide a high response speed.

Kondo et al., in contrast, teaches a compound semiconductor light-emitting layer of nitride. But, it does not teach or suggest a structure for increasing response speed. (In other words, the light-emitting layer of Kondo et al. merely has a nitride layer for obtaining an efficient luminous intensity.)

Furthermore, the semiconductor light-emitting device of <u>Iwata</u> has a plurality of semiconductor thin chips 14 as a structure for obtaining high light-emitting efficiency, with each

ATTORNEY DOCKET NO. 046124-5240

Application No.: 10/679,517

Page 7

of the semiconductor thin chips 14 having a confinement structure such that an active layer 13 with a quantum well and cladding layer 12 for further increasing light-emitting efficiency.

However, the structure of <u>Iwata</u> does not increase response speed because the active layer 13 of each semiconductor thin chip is confined with the cladding layers 12 and the semiconductor thin chips are laminated in multiple stages.

Thus, as neither <u>Iwata</u> nor <u>Kondo et al.</u> teach or suggest increasing response speed,

Applicants submit that there is no motivation to combine these references in the manner suggested by the Examiner. Accordingly, the claims are all believed to be patentably distinguishable over the applied references of record. Reconsideration and withdrawal of the pending rejections is therefore respectfully requested.

ATTORNEY DOCKET NO. 046124-5240

Application No.: 10/679,517

Page 8

CONCLUSION

In view of the foregoing, Applicants submit that the pending claims are in condition for

allowance, and respectfully request reconsideration and the timely allowance of the pending

claims. Should the Examiner feel that there are any issues outstanding after consideration of this

response, the Examiner is invited to contact Applicants undersigned representative to expedite

prosecution. A favorable action is awaited.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby

authorized by this paper to charge any additional fees during the entire pendency of this

application including fees due under 37 C.F.R. § 1.16 and 1.17 which may be required, including

any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0310.

This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF**

TIME in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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